

## CLAIMS

We claim:

- 1 1. A behavior processor system for operating a portion of a user design and interfacing with  
2 a host testbench process, comprising:  
3 a reprogrammable logic element for modeling a hardware model of the portion of the user  
4 design that includes a behavior level function; and  
5 a testbench call back process for responding to the behavior level function in the  
6 reprogrammable logic element by sending a signal to the host testbench process.
- 1 2. The system of claim 1, wherein the behavior level function includes a condition.
- 1 3. The system of claim 1, wherein the behavior level function includes a condition and the  
2 occurrence of the condition triggers the testbench call back process.
- 1 4. The system of claim 2, wherein the condition includes an “if-then” conditional statement  
2 implemented in hardware.
- 1 5. The system of claim 1, wherein the signal includes an interrupt from the testbench call  
2 back process to the host testbench process.
- 1 6. The system of claim 1, wherein the signal includes an interrupt from the reprogrammable  
2 logic element to the host testbench process.
- 1 7. The system of claim 1, wherein the signal includes data from the testbench call back  
2 process to the host testbench process.

- 1 8. The system of claim 2, wherein the reprogrammable logic element temporarily suspends  
2 operation upon the occurrence of the condition.
- 1 9. The system of claim 8, wherein the reprogrammable logic element resumes operation from  
2 the point at which operation was temporarily suspended upon the service of the signal by the host  
3 testbench process.
- 1 10. The system of claim 2, wherein the reprogrammable logic element temporarily pauses  
2 operation upon the occurrence of the condition.
- 1 11. The system of claim 1, wherein the reprogrammable logic element includes a clock that  
2 controls the speed of processing instructions and data in the reprogrammable logic element.
- 1 12. The system of claim 11, wherein the clock runs at 20 MHz.
- 1 13. A verification system for analyzing a user design, comprising:  
2 a host workstation for modeling and operating a software model of the user design;  
3 a reprogrammable hardware emulator for modeling a first hardware model of at least a  
4 portion of the user design; and  
5 a behavior processor for modeling a second hardware model of a selected portion of the  
6 user design.
- 1 14. The verification system of claim 13, wherein the selected portion includes a behavioral  
2 aspect of the user design.
- 1 15. The verification system of claim 13, wherein the selected portion includes at least one  
2 condition in the user design.
- 1 16. The verification system of claim 15, wherein the at least one condition includes an “if-

2 then” conditional statement.

1 17. The verification system of claim 13, wherein the behavior processor includes a testbench  
2 callback process for responding to the selected portion of the user design modeled in the  
3 reprogrammable hardware emulator by sending a signal to the host workstation.

1 18. The verification system of claim 15, wherein the behavior processor includes a testbench  
2 callback process for responding to the occurrence of the condition in the reprogrammable  
3 hardware emulator by sending a signal to the host workstation.

1 19. The verification system of claim 18, wherein the reprogrammable hardware emulator  
2 temporarily suspends operation upon the occurrence of the condition.

1 20. The verification system of claim 19, wherein the reprogrammable hardware emulator  
2 resumes operation from the point at which operation was temporarily suspended upon the service  
3 of the signal by the host workstation.

1 21. The verification system of claim 18, wherein the reprogrammable hardware emulator  
2 temporarily pauses operation upon the occurrence of the condition.

1 22. The verification system of claim 19, wherein the behavior processor sends a wait signal to  
2 the reprogrammable hardware emulator upon the occurrence of the condition so that the  
3 reprogrammable hardware emulator temporarily suspends operation.

1 23. The verification system of claim 22, wherein the behavior processor sends a resume signal  
2 to the reprogrammable hardware emulator upon the service of the signal by the host workstation  
3 so that the reprogrammable hardware emulator resumes operation from the point at which  
4 operation was temporarily suspended.

- 1 24. The verification system of claim 22, wherein the behavior processor toggles the wait  
2 signal to the reprogrammable hardware emulator upon the service of the signal by the host  
3 workstation so that the reprogrammable hardware emulator resumes operation from the point at  
4 which operation was temporarily suspended.
- 1 25. The verification system of claim 13, wherein the behavior processor operates when it  
2 receives a request for service from the host workstation.
- 1 26. The verification system of claim 13, wherein the behavior processor operates when it  
2 receives a request for service from the reprogrammable hardware emulator.
- 1 27. A method of verifying a user design where the verification environment includes a host  
2 workstation for running a simulation of the user design and a testbench process, comprising steps:  
3 modeling a behavioral portion of the user design in hardware, where the behavioral  
4 portion includes a service request; and  
5 sending a signal to the testbench process in the host upon the occurrence of the service  
6 request.
- 1 28. The method of claim 27, further comprising step:  
2 suspending the operation of the simulation until the host workstation services the signal.
- 1 29. The method of claim 27, further comprising step:  
2 suspending the operation of the simulation until the testbench process services the signal.
- 1 30. The method of claim 27, wherein the step of modeling the behavioral portion includes  
2 modeling conditional statements.
- 1 31. The method of claim 28, wherein the step of modeling the conditional statements includes  
2 "if-then" statements.

1 32. A method of verifying a user design where the verification environment includes a host  
2 workstation for running a simulation of the user design and a testbench process, comprising steps:  
3 modeling a conditional portion of the user design in a hardware environment;  
4 executing the conditional portion in the hardware environment; and  
5 sending an interrupt to the testbench process in the host upon the occurrence of at least  
6 one condition in the conditional portion.

1 33. The method of claim 32, further comprising step:  
2 suspending the operation of the simulation until the host workstation services the  
3 interrupt.

1 34. The method of claim 32, further comprising step:  
2 suspending the operation of the simulation until the testbench process services the  
3 interrupt.

1 35. The method of claim 32, wherein the step of modeling the conditional statements includes  
2 "if-then" statements.

1 36. The method of claim 32, wherein the step of executing occurs at the speed of a hardware  
2 clock.

1 37. The method of claim 36, wherein the step of executing occurs at 20 MHz.